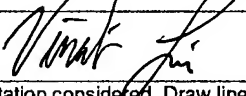


Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-304US1	Application No. 10/069,195
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	
		Filing Date November 7, 2002	Group Art Unit 2181

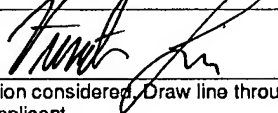
(37 CFR §1.98(b))

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
W	AA	2002/0038403	03/2002	Wolrich et al.			
W	AB	3,881,173	04/1975	Larsen et al.			
W	AC	4,454,595	06/1984	Cage			
W	AD	4,477,872	10/1984	Losq et al.			
W	AE	4,569,016	02/1986	Hao et al.			
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W	AK	4,868,735	09/1989	Moller et al.			
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W	AM	5,045,995	09/1991	Levinthal et al.			
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W	AO	5,165,025	11/1992	Lass			
W	AP	5,170,484	12/1992	Grondalski			
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W	AW	5,394,530	02/1995	Kitta			
W	AX	5,428,779	06/1995	Allegrucci et al.			
W	AY	5,450,603	09/1995	Davies			
W	AZ	5,463,746	10/1995	Brodnax et al.			
W	BA	5,509,130	04/1996	Trauben et al.			

Examiner Signature 	Date Considered 5-2-2007
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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W	BB	5,541,920	07/1996	Angle et al.			
W	BC	5,544,337	08/1996	Beard et al.			
W	BD	5,572,690	11/1996	Molnar et al.			
W	BE	5,600,848	02/1997	Sproull et al.			
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W	BI	5,680,564	10/1997	Divivier et al.			
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W	BK	5,724,563	03/1998	Hasegawa			
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W	BY	5,898,866	04/1999	Atkins et al.			
W	BZ	5,900,025	05/1999	Sollars			
W	CA	5,923,872	07/1999	Chrysos et al.			
W	CB	5,926,646	07/1999	Pickett et al.			

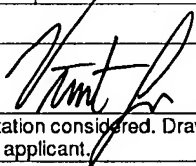
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(37 CFR §1.98(b))

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
W	CC	5,928,358	07/1999	Takayama et al.			
W	CD	5,937,177	08/1999	Molnar et al.			
W	CE	5,943,491	08/1999	Sutherland et al.			
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W	CW	6,223,277	04/2001	Karguth			
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W	DB	6,269,391	07/2001	Gillespie			
W	DC	6,275,508	08/2001	Aggarwal et al.			

Examiner Signature



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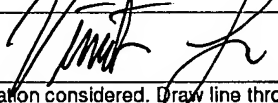
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	Applicant Gilbert Wolrich et al.		
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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
W	DD	6,279,066	08/2001	Velingker			
W	DE	6,314,510	11/2001	Saulsbury et al.			
W	DF	6,338,133	01/2002	Schroter			
W	DG	6,378,124	04/2002	Bates et al.			
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W	DL	6,496,847	12/2002	Bugnion et al.			
W	DM	6,505,229	01/2003	Turner et al.			
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W	DP	6,560,629	05/2003	Harris			
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W	DS	6,574,702	06/2003	Khanna et al.			
W	DT	6,697,935	02/2004	Borkenhagen et al.			
W	DU	6,862,676	03/2005	Knapp et al.			
W	DV	6,976,095	12/2005	Wolrich et al.			
W	DW	6,983,350	01/2006	Adiletta et al.			
W	DX	7,020,871	03/2006	Bernstein et al.			

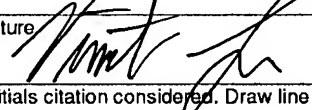
Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
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W	DY	0 130 381	01/1985	Europe				
W	DZ	0 463 855	01/1992	Europe				
W	EA	0 476 628	03/1992	Europe				

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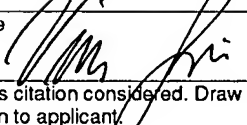
Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
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W	EB	0 696 772	02/1996	Europe				
W	EC	59-111533	06/1984	Japan (abstract only)				X
W	ED	WO03/019399	03/2003	WIPO				
W	EE	WO03/085517	10/2003	WIPO				

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W	EF	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
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W	EH	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", <i>IEEE</i> , pp. 57-62, (1996).
W	EI	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
W	EJ	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
W	EK	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
W	EL	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
W	EM	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM & IEEE-CS</i> , 20(2):136-145, May 1992.
W	EN	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
W	EO	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).
W	EP	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , <i>IEEE</i> , pp. 26-31 (1996).
W	EQ	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
W	ER	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
W	ES	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
W	ET	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).

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Examiner Initial	Desig. ID	Document
W	EU	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
W	EV	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27th Annual Hawaiian International Conference on System Sciences, IEEE</i> , pp. 584-593, (1994).
W	EW	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
W	EX	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
W	EY	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
W	EZ	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
W	FA	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

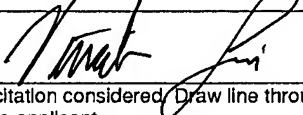
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W	AA	5,860,085	01/1999	Stormon et al.			
W	AB	6,052,769	04/2000	Huff et al.			
W	AC	6,934,951	08/2005	Wilkinson, III et al.			
W	AD	7,181,594	02/2007	Wilkinson, III et al.			
W	AE	7,191,309	03/2007	Wolrich et al.			
	AF						
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	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
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	AL							
	AM							
	AN							
	AO							
	AP							

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Examiner Initial	Desig. ID	Document
W	AQ	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 69-71, (1997).
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	AS	
	AT	

Examiner Signature 	Date Considered 5-8-07
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